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HARMONIC ELIMINATION IN MULTILEVEL INVERTER

[1]Romesh Kumar Jyoti, [2]Ashish Choubey

[1]M.E. Student, [2]Assistant Professor
Departent of Electrical Engineering
JEC, Jabalpur, M.P, India

Abstract: **Power quality is very important aspect in power system. The harmonics in power system are produced by various electronic devices. Conventional inverters produce more harmonics and distortions in power system which can be reduced by filters with increase in size and cost. Multilevel inverter reduces the harmonic contents and achieves sinusoidal signals without extra circuitry. For output step-pulse waveform, it is necessary to obtain the conducting angles of switching devices. The predominant lower-order harmonics can be eliminated. In this paper simulation of 5-level inverter for lagging power factor load is done and by using constant-K filter the output voltage and current harmonic distortion is analysed at different combination of conduction angles. A comparative performance of filter is also presented for different values of filter cut-off frequency.**

Keywords: **Multilevel Inverter, Conduction angle, Harmonic distortion, Harmonic factor, Filter, Cut-off frequency.**

I. INTRODUCTION

The cascaded H-bridge inverter has drawn tremendous interest due to great demand of medium-voltage high-power inverters. The cascaded inverter uses series string of single-phase full-bridge inverters to construct multilevel phase legs with separate DC sources. A single H-bridge is shown in figure 3.3. The output of each H-bridge can have three discrete levels, results in a staircase waveform that is nearly sinusoidal even without filtering. A single H-bridge is a three-level inverter. Each single-phase full bridge inverter generates three voltages at the output: $+V_{dc}$, 0 and $-V_{dc}$. Figure1 shows a single phase five level cascaded H-bridge cell inverter realized by connecting two three level conventional full bridge inverters in series.

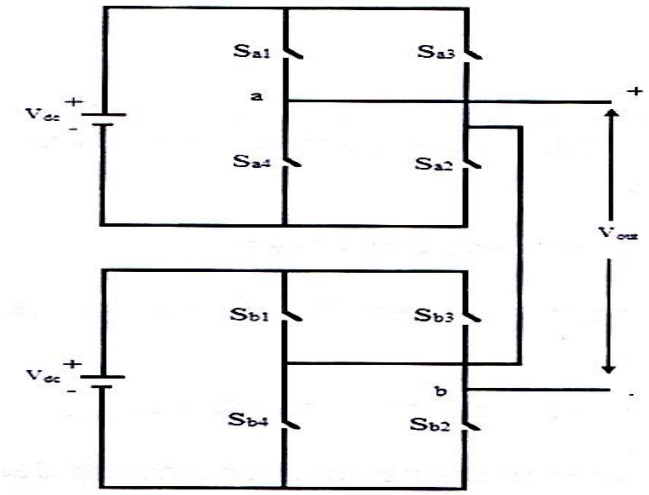

Fig. 1 Cascaded (5-Level) Inverter Topology

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Switch pairs (S1 & S3) and (S2 & S4) are c0mplementary to each other. The different voltage levels that can be obtained at the output terminals are $+2V_{dc}$, $+V_{dc}$, 0 , $-V_{dc}$. and $-2V_{dc}$. If the DC voltage sources in both the inverter circuits connected in series are not equal to each other, then nine levels can be obtained at the output terminals. The number of levels in the output voltage can be increased by two by adding an identical inverter in series. The n number of output phase voltage levels in a cascaded inverter with s separate DC sources is (n= 2S+1) possible levels. Cascaded H-bridge cell inverters use the least number of power electronics devices when compared to any other topology. However, they require isolated power sources in each cell which in turn requires a large isolation transformer.The advantages of cascaded H-bridge multilevel inverter are the followings:

- The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.
- No extra clamping diodes or voltage balancing capacitors are needed.
- Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of the output of each bridge.

II. SIMULINK MODEL

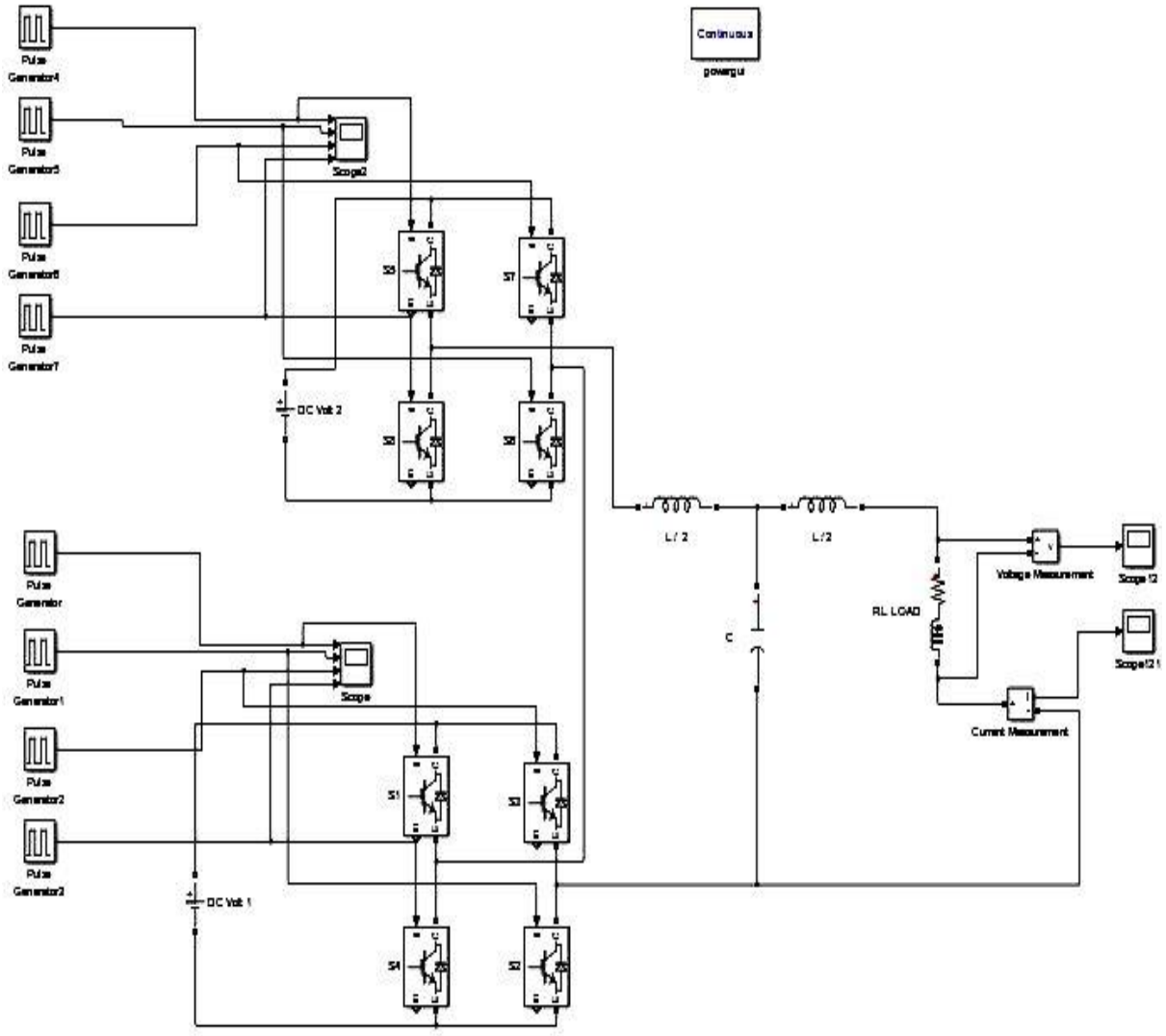

Fig. 2 Simulink model of 5-level inverter

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III. RESULTS

Table1. THD of output voltage and current under different combinations of conduction angles in 5-level inverter for lagging pf load (6+j8)Ω

α_2	$\alpha_1 = 5^0$		$\alpha_1 = 10^0$		$\alpha_1 = 15^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%V_{THD}$	$\%V_{THD}$	$\%I_{THD}$
55^0	23.34	21.65	19.05	20.86	19.7	20.11
50^0	21.03	21.5	18.36	19.77	19.07	20.06
45^0	19.36	20.66	16.91	19.81	17.22	20.08
40^0	19.2	21.73	17.17	21	17.11	19.31
35^0	21.31	22.19	17.13	20.43	18.74	19.71
30^0	21.16	21.95	19.53	21.08	20.57	20.29
25^0	24.1	23.63	22.47	21.92	24.26	22.09
20^0	28.41	24.49	28.69	23.79	30.68	22.87
15^0	31.99	24.68	29.72	24.61	-	-
10^0	35.39	26.44	-	-	-	-

α_2	$\alpha_1 = 20^0$		$\alpha_1 = 25^0$		$\alpha_1 = 30^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%V_{THD}$	$\%V_{THD}$	$\%I_{THD}$
55^0	22.54	20.01	26.25	19.06	32.45	20.74
50^0	19.95	18.69	24.69	20.07	28.8	19.47
45^0	18.87	18.84	24.03	19.98	28.22	20.19
40^0	18.21	20.15	24.51	19.83	29.93	20.09
35^0	20.41	20.3	23.25	20.05	30.68	19.89
30^0	23.52	20.88	25.16	20.2	-	-
25^0	26.71	21.3	-	-	-	-

Table2. Output current harmonic profile (% harmonics) for different value of α_2 when $\alpha_1 = 20^0$ in 5-level inverter for lagging pf load (6 + j8) Ω

Harmonic Order	$\alpha_1 = 20^0$			
	$\alpha_2 = 55^0$	$\alpha_2 = 50^0$	$\alpha_2 = 45^0$	$\alpha_2 = 40^0$
	$\%I_{THD} = 20.01$	$\%I_{THD} = 18.69$	$\%I_{THD} = 18.84$	$\%I_{THD} = 20.15$
DC	16.3	15.33	15.36	16.65
3	9.64	8.5	8.16	8.16
5	5.02	5.14	5.83	6.88
7	3.52	3.34	3.46	4.19
9	4.13	3.09	2.94	2.88
11	3.06	2.71	2.83	2.68
13	1.88	1.87	2.16	2.65
15	1.89	1.61	1.71	2.12
17	1.74	1.52	1.67	1.49

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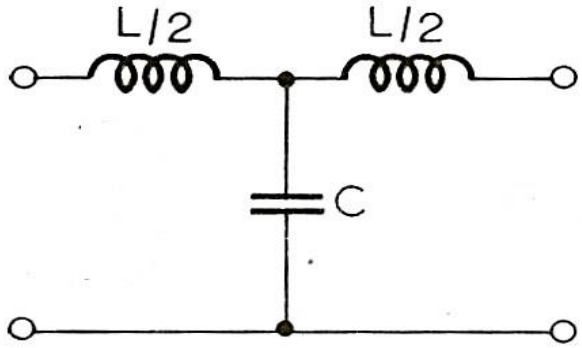
Harmonic Order	$\alpha_1 = 20^0$		
	$\alpha_2 = 35^0$	$\alpha_2 = 30^0$	$\alpha_2 = 25^0$
	$\%I_{THD} = 20.3$	$\%I_{THD} = 20.88$	$\%I_{THD} = 21.3$
DC	16.84	17.16	17.34
3	8.1	8.51	9.36
5	6.83	6.7	6.04
7	4.69	5.25	5.23
9	3.11	3.54	3.91
11	2.47	2.5	2.78
13	2.29	2.06	2.06
15	2.09	1.99	1.66
17	1.75	2.04	1.55

Design of constant k low-pass filter:



If the load impedance is R = 10 Ω then for cut-off frequency $f_{cut-off} = 50\ Hz$, 150 Hz and 300 Hz filter components are different.

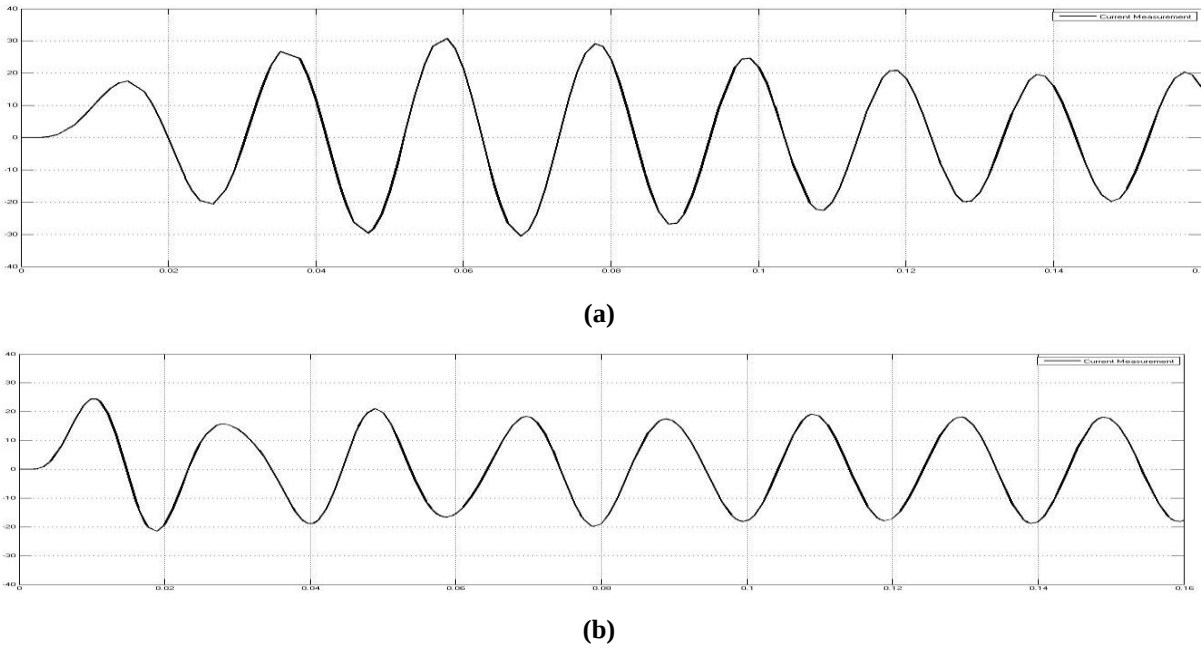
$\boldsymbol{f_{cut-off} = 50\ Hz}$ **:-** $L = .0636\ henery\ \ C = 636\ \mu\ farad$

$\boldsymbol{f_{cut-off} = 100\ Hz}$ **:-** $L = .0318\ henery\ \ C = 318\ \mu\ farad$

$\boldsymbol{f_{cut-off} = 300\ Hz}$ **:-** $L = .0106\ henery\ \ C = 106\ \mu\ farad$

Table 3. THD analysis of output current (% harmonics) for resistive load in 5-level Inverter with and without constant-K filter at different cut-off frequency of filter

Harmonic Order	$\alpha_1 = 5^0$ and $\alpha_2 = 45^0$			
	Without constant K filter	With constant K filter		
		$f_{cut-off} = 50\ Hz$	$f_{cut-off} = 100\ Hz$	$f_{cut-off} = 300\ Hz$
	$\%I_{THD} = 18.17$	$\%I_{THD} = 14.05$	$\%I_{THD} = 14.22$	$\%I_{THD} = 9.73$
DC	2.43	7.4	1.51	0.39
3	4.4	0.34	2.03	5.3
5	1.24	0.75	1.13	2.73
7	11.06	0.2	0.58	5.8
9	7.31	0.23	0.91	1.56
11	3.2	0.11	0.28	0.25
13	3.09	0.09	0.55	0.2
15	1.5	0.13	0.32	0.55
17	3.28	0.05	0.45	0.48



(a)

(b)

Fig. 3 Output current waveform of 5-level inverter at different cut-off frequency (a) 50 Hz (b) 100 Hz

IV. CONCLUSIONS

From table 3 it is clear thaof output current of 5-level inverter is minimised by constant-K low pass filter at different cut-off frequency. Wave shape shows initially oscillations in current and after 2-3 cycles it settles down as a sine wave.

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